Reg. No. | | | | | | | | | | | | |

Question Paper Code : 27156

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Second Semester

Computer Science and Engineering

CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(126)_{10}$ to octal number and binary number.
2. Write short notes on weighted binary codes.
3. Discuss NOR operation with a truth table.
4. Draw the truth table of half adder.
5. Write short notes on propagation delay.
6. Draw the diagram of T flip flop and discuss its working.
7. What is a shift register?
8. What is a race condition?
9. What is memory address register?
10. Write short notes on PLA.

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following switching functions using Karnaugh map method and realize expression using gates $F(A,B,C,D) = \Sigma(0,3,5,7,8,9,10,12,15)$. (16)

Or

(b) Simplify the following switching functions using Quine McCluskey's tabulation method and realize expression using gates $F(A,B,C,D) = \Sigma(0,5,7,8,9,10, 11, 14,15)$. (16)

12. (a) Design a full subtractor and derive expression for difference and borrow. Realize using gates. (16)

Or

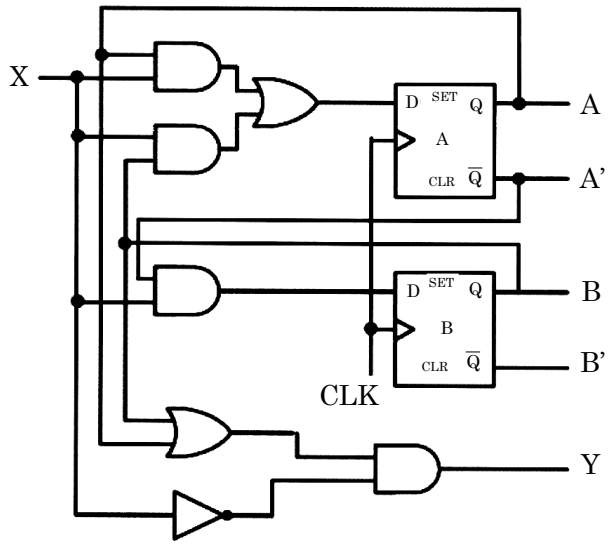
(b) Design a code converter that converts a 8421 to BCD code. (16)

13. (a) Design a sequence detector that detects a sequence of three or more consecutive 1 's in a string of bits coming through an input line and produces an output whenever this sequence is detected. (16)

Or

(b) Design a three bit synchronous counter with T flip flop and draw the diagram. (16)

14. (a) Analyze the following clocked sequential circuit and obtain the state equations and state diagram. (16)



Or

(b) Design a serial adder using a full adder and a flip flop. (16)

15. (a) Implement the following function using PAL F1 (A, B, C) = $\Sigma(1,2,4,6)$; F2 (A, B, C) = $\Sigma(0,1,6,7)$; F3 (A, B, C) = $\Sigma(1,2,3,5,7)$. (16)

Or

(b) Design a combinational circuit using ROM that accepts a three bit binary number and outputs a binary number equal to the square of the input number. (16)

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Question Paper Code : 57234

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2016

Second Semester

Computer Science and Engineering

CS 6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three Hours **Maximum : 100 Marks**

Answer ALL questions.

PART – A (10 × 2 = 20 Marks)

1. Find the Octal equivalent of the hexadecimal number DC.BA.
2. What is meant by multilevel gates network ?
3. Define Combinational circuits.
4. Design the combinational circuit with 3 inputs and 1 output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
5. State the excitation table of JK-Flip Flop.
6. A seven bit Hamming code is received as 1111110. What is the correct code ?
7. What is the minimum number of flip flops needed to build a counter of modulus 8 ?
8. What is lockout ? How it is avoided ?
9. Define the critical rate and non critical rate.
10. Draw the wave forms showing static 1 hazard ?

PART – B (5 × 16 = 80 Marks)

11. (a) Reduce the expression using Quine McCluskey method.

$F(x_1, x_2, x_3, x_4, x_5) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 14, 17, 18, 21, 29, 31) + \sum d(11, 20, 22)$ **(16)**

OR

(b) Determine the MSP form of the Switching function F (a, b, c, d) = _ (0, 2, 4, 6, 8) + _d(10, 11, 12, 13, 14, 15). **(16)**

12. (a) Design a full adder with inputs *x*, y, z and two outputs S and C. The circuits performs *x* + y + z, z is the input carry, C is the output carry and S is the Sum. **(16)**

OR

(b) Design a logic circuit that accepts a 4-bit Grey code and converts it into 4-bit binary code. **(16)**

13. (a) Implement the following Boolean function with a 4 × 1 multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D these values are obtained by expressing F as a function of C and D for each of the four cases when AB = 00, 01, 10 and 11. These functions may have to be implemented with external gates. F(A, B, C, D) = ∑ (1, 2, 5, 7, 8, 10, 11, 13, 15). **(16)**

OR

(b) Draw a neat sketch showing implementation of Z_1 = ab'd'e + a'b'c' e + bc + de, Z_2 = a'c'e, Z_3 = bc + de +c'd'e + bd and Z_4 = a'c'e + ce using a 5*8*4 PLA. **(16)**

14. (a) Design a binary counter using T flip-flops to count in the following sequences :

(i) 000, 001, 010, 011, 100, 101, 111, 000

(ii) 000, 100, 111, 010, 011, 000 **(16)**

OR

(b) Design a modulo 5 synchronous counter using JK Flip Flop and implement it. Construct its timing diagram. **(16)**

15. (a) Design an asynchronous sequential circuit with 2 inputs X and Y and with one output Z Wherever Y is 1, input X is transferred to Z. When Y is 0; the output does not change for any change in X. Use SR latch for implementation of the circuit. **(16)**

OR

(b) Discuss in detail the procedure for reducing the flow table with an example. **(16)**

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Question Paper Code : 71671

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Classify the logic families by its operations.
2. State and prove the consensus theorem.
3. What is priority encoder?
4. Draw the circuit for 2-to-1 line multiplexer.
5. What are the significances of state assignment?
6. Write any two applications of shift register.
7. Define race around condition.
8. What is edge triggered flip flop?
9. List the major differences between PLA and PAL.
10. What is memory decoding?

PART B — (5 × 16 = 80 marks)

11. (a) Using Tabulation method simplify the Boolean function

F (w,x,y,z) = $\sum$(1,2,3,5,9,12,14,15) which has the don't care conditions d(4,8,11). (16)

Or

(b) Simplify the following expression :

$y = m_1 + m_3 + m_4 + m_7 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{14}$ using

(i) Karnaugh Map

(ii) Quine McClusky method. (16)

12. (a) Construct a BCD adder circuit and write a HDL program module for the same. (16)

Or

(b) Implement the Boolean function using 8:1 multiplexer F(W,X,Y,Z) = W'XZ'+ WYZ + X'YZ + W'Y'Z. (16)

13. (a) Implement T-flip flop and JK flip flop using D flip flop. (16)

Or

(b) Design and implement Mod-5 Synchronous Counter using JK flip flop and also draw the timing diagram. (16)

14. (a) Summarize the design procedure for asynchronous sequential circuit. (16)

Or

(b) Explain the different types of hazards that occurs in asynchronous sequential circuits and Combinational circuits. (16)

15. (a) Design a 16 bit RAM array (4×4 RAM) and explain the operation. (16)

Or

(b) Explain the following :

(i) ASIC (8)

(ii) Field Programmable Gate Array. (8)

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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 77091

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(0.6875)_{10}$ to binary.

2. Prove the following using DeMorgan's theorem.

$$\left[(x+y)' + (x+y)'\right]' = x + y .$$

3. Implement a full adder with 4 × 1 Multiplexer.

4. Write the Data flow description of a 4-bit Comparator.

5. Give the block diagram of Master- Slave D flip-flop.

6. What is a Ring counter?

7. Compare asynchronous and synchronous sequential circuit.

8. What is a critical race condition? Give example.

9. Differentiate between EEPROM and PROM.

10. How to detect double error and correct single error?

PART B — (5 × 16 = 80 marks)

11. (a) Simplify the following Boolean expression in

(i) Sum-of-product

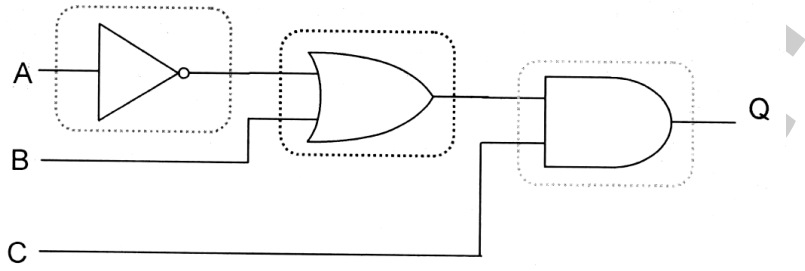
(ii) Product-of-sum using Karnaugh-map (16)

AC' + B'D + A'CD + ABCD

Or

(b) (i) Express the following function in sum of min-terms and product of max-terms $F(x, y, z) = x + yz$. (8)

(ii) Convert the following logic system into NAND gates only. (8)



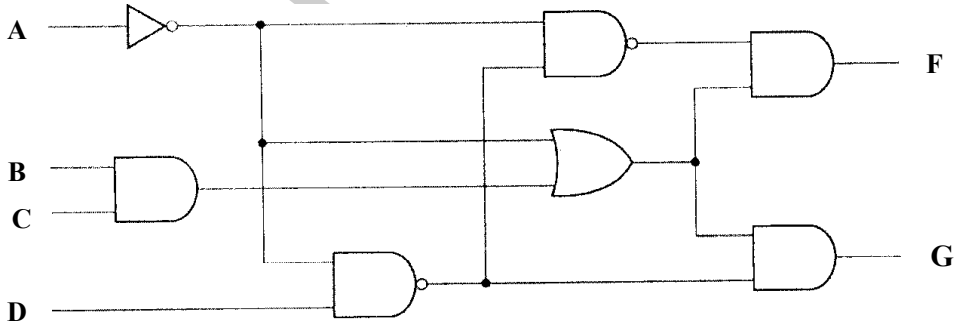
12. (a) (i) Implement the following Boolean functions with a multiplexer :

$F(w, x, y, z) = \sum (2, 3, 5, 6, 11, 14, 15)$. (8)

(ii) Construct a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoder. (8)

Or

(b) (i) Explain the Analysis procedure. Analyze the following logic diagram. (8)



(ii) With neat diagram explain the 4-bit adder with carry lookahead. (8)

13. (a) (i) A sequential circuit with two D flip-flops A and B, one input x, and one output z is specified by the following next-state and output equations :

$A(t + 1) = A' + B$, $B(t + 1) = B'x$, $z = A + B'$

(1) Draw the logic diagram of the circuit. (4)

(2) Derive the state table. (3)

(3) Draw the state diagram of the circuit. (3)

(ii) Explain the difference between a state table, characteristic table and an excitation table. (6)

Or

(b) Consider the design of a 4-bit BCD counter that counts in the following way :

0000, 0010, 0011, ..., 1001 and back to 0000.

(i) Draw the state diagram. (4)

(ii) List the next state table. (4)

(iii) Draw the logic diagram of the circuit. (8)

14. (a) (i) Explain the Race-free state assignment procedure. (8)

(ii) Reduce the number of states in the following state diagram. Tabulate the reduced state table and draw the reduced state diagram. (8)

Present state	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

Or

(b) Explain the hazards in combinational circuit and sequential circuit and also demonstrate a hazard and its removal with example. (16)

15. (a) (i) Write short note on Address multiplexing. (8)

(ii) Briefly discuss the sequential programmable devices. (8)

Or

(b) (i) Implement the following two Boolean functions with a PLA. (10)

F1 = A B' + A C + A' B C'

F2 = (AC + BC)'

(ii) Give the Internal block diagram of 4 X4 RAM. (6)

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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 80285

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2016.

Second Semester

Computer Science and Engineering

CS 6201 — DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the principle of duality.

2. State and prove the Consensus Theorem.

3. What is priority encoder?

4. Draw the circuit for 2-to-1 multiplexer.

5. What is the operation of JK flip flop?

6. Define race around condition.

7. Define flow table in asynchronous sequential circuit.

8. What are races?

9. How to detect double error and correct single error?

10. Give the comparison between EPROM and PLA.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Minimize the following expression using Karnaugh map. (8)

Y = A' BC'D' + A'BC'D + ABC'D' + A'B'CD'

(ii) State and prove the Demorgan's theorem. (8)

Or

(b) (i) Implement the switching function $f(x, y, z) = \sum m(0, 1, 3, 4, 12, 14, 15)$ with NAND gates. (8)

(ii) Minimize the following expression using Quine Mccluskey method.

Y = A'BC'D' + A' BC'D + ABC'D' + ABC'D +AB'C'D + A'B'CD'. (8)

12. (a) (i) Compare and contrast between encoder and multiplexer. (8)

(ii) Design a combinational circuit to convert binary to gray code. (8)

Or

(b) (i) Design a combinational circuit that converts 8421 BCD code to excess-3 code. (8)

(ii) With neat diagram explain the 4 bit adder with carry look ahead. (8)

13. (a) (i) Implement JK flip flop using D flip flop. (8)

(ii) How the race condition can be avoided in a flip flop? (8)

Or

(b) Consider the design of 4-bit BCD counter that counts in the following way:

0000, 0001, 0010...., 1001 and back to 0000. Draw the logic diagram of this circuit. (16)

14. (a) Explain the steps for design of asynchronous sequential circuits. (16)

Or

(b) Explain the types of hazards in combinational circuits and sequential circuits and also demonstrate a hazard and its removal with example. (16)

15. (a) Implement the following using PLA.

$A\ (x, y, z) = \sum m\ (1, 2, 4, 6)$

$B\ (x, y, z) = \sum m\ (0, 1, 6, 7)$

$C\ (x, y, z) = \sum m\ (2, 6)$. (16)

Or

(b) Discuss on the concept of working and applications of semiconductor memories. (16)

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